UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,753	12/03/2001	Shoab Ahmad Khan	0037203-7	8281

29484 7590 03/25/2005

PATENTMETRIX
14252 CULVER DR. BOX 914
IRVINE, CA 92604

EXAMINER	
CERVETTI, DAVID GARCIA	

ART UNIT	PAPER NUMBER
2136	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,753	KHAN ET AL.	
	Examiner	Art Unit	
	David G. Cervetti	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The listing of references in the specification (page 2, lines 10-11) is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 1370a (page 28, line 9), 1330 (page 28, line 32), 1331 (page 29, line 3), 1332 (page 29, line 6). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The disclosure is objected to because of the following informalities: “DMA” (page 3, line 19), “DTMF” (page 29, line 12). While well known in the art, these terms have not been defined.

The disclosure is objected to because of the following informalities: a brief description of Figure 13b is missing.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 12-16, 19-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Parameswaran Nair et al. (US Patent Number: 5,724,356).

Regarding claim 1, Parameswaran Nair et al. teach a media processor for the processing of media based upon instructions (column 6, lines 1-8), comprising: a plurality of processing layers wherein each processing layer has at least one processing unit (column 5, lines 53-57), at least one program memory (column 5, lines 53-57), and at least one data memory (column 6, lines 10-20, column 8, lines 48-61), each of said processing unit, program memory, and data memory being in communication with one another (column 5, lines 57-64); at least one processing unit in at least one of said processing layers performing line echo cancellation functions on received data (column 6, lines 1-8); at least one processing unit in at least one of said processing layers performing encoding or decoding functions on received data (column 6, lines 1-8); and a task scheduler adapted to receive a plurality of tasks from a source and distributing said tasks to said processing layers (column 25, lines 24-38).

Regarding claim 2, Parameswaran Nair et al. teach further comprising a direct memory access controller for handling data transfers, each of said transfers having a

size and a direction, from at least one data memory having an address and a plurality of external memory units, each having an address (column 19, lines 15-50).

Regarding claim 3, Parameswaran Nair et al. teach wherein said transfers between at least one data memory and at least one external memory occur by utilizing the address of the data memory, the address of the external memory, the size of the transfer, and the direction of the transfer (column 19, lines 15-50).

Regarding claim 4, Parameswaran Nair et al. teach wherein the task scheduler is in communication with an external memory (column 25, lines 24-38, 49-59).

Regarding claim 5, Parameswaran Nair et al. teach the media processor of claim 1, further comprising an interface for the receipt and transmission of data and control signals (column 5, lines 40-65).

Regarding claim 12, Parameswaran Nair et al. teach a media gateway for the processing of data and communication of data across a plurality of networks (column 3, lines 40-65), comprising: a plurality of media processors, each of said media processors having a plurality of processing layers wherein each processing layer has at least one processing unit (column 5, lines 53-57), at least one program memory (column 5, lines 53-57), and at least one data memory (column 6, lines 10-20, column 8, lines 48-61), each of said processing unit, program memory, and data memory being in communication with one another (column 5, lines 57-64), wherein at least one processing unit in at least one of said processing layers performs echo cancellation functions on received data (column 6, lines 1-8), wherein at least one processing unit in at least one of said processing layers performs encoding or decoding functions on

received data (column 6, lines 1-8), and wherein a task scheduler is adapted to receive a plurality of tasks from a source and distribute said tasks to the processing layers (column 5, lines 53-65); a plurality of packet processors in communication with at least one of said media processors wherein the packet processor is adapted to packetize processed data (column 9, lines 5-25); and a host processor in communication with at least one said packet or media processors (column 7, lines 25-45).

Regarding claim 13, Parameswaran Nair et al. teach a method for processing media based upon instructions (column 6, lines 1-8), comprising the steps of: receiving said media through a data interface (column 25, lines 24-38); scheduling the processing of said media through a task scheduler adapted to receive a plurality of tasks from a source and distributing said tasks to a plurality of processing layers (column 25, lines 24-38); and processing said media in the plurality of processing layers wherein each processing layer has at least one processing unit (column 5, lines 53-57), at least one program memory (column 5, lines 53-57), and at least one data memory (column 6, lines 10-20, column 8, lines 48-61), each of said processing unit, program memory, and data memory being in communication with one another (column 5, lines 57-64).

Regarding claim 14, Parameswaran Nair et al. teach wherein said processing step further comprises performing echo cancellation functions on received data (column 6, lines 1-8).

Regarding claim 15, Parameswaran Nair et al. teach wherein said processing step further comprises performing encoding or decoding functions on received data (column 6, lines 1-8).

Regarding claim 16, Parameswaran Nair et al. teach wherein the processing step occurs in parallel across multiple processing layers, each of said processing layers having similar processing units (column 8, lines 1-37).

Regarding claim 19, Parameswaran Nair et al. teach a processor (column 6, lines 1-8) for the processing of data based upon instructions, comprising: a plurality of processing layers wherein each processing layer has at least one processing unit (column 5, lines 53-57), at least one program memory (column 5, lines 53-57), and at least one data memory (column 6, lines 10-20, column 8, lines 48-61), each of said processing unit, program memory, and data memory being in communication with one another (column 5, lines 57-64); and a task scheduler adapted to receive a plurality of tasks from a source and distributing said tasks to the processing layers (column 25, lines 24-38).

Regarding claim 20, Parameswaran Nair et al. teach wherein at least one of said plurality of processing layers comprises a processing unit performing echo cancellation functions on received data (column 6, lines 1-8).

Regarding claim 21, Parameswaran Nair et al. teach wherein at least one of said plurality of processing layers comprises a processing unit performing encoding or decoding functions on received data (column 6, lines 1-8).

Regarding claim 22, Parameswaran Nair et al. teach wherein the plurality of processing layers communicate with the task scheduler through a controller interface (column 5, lines 53-65).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 18 is rejected under 35 U.S.C. 102(e) as being anticipated by Kundu et al. (US Patent Number: 6,751,723).

Regarding claim 18, Kundu et al. teach a distributed processing system implemented on a single chip having a total memory capacity comprising: at least two processing layers (column 4, lines 20-37) wherein each processing layer has at least one processing unit (column 4, lines 25-26, logic clusters) and a plurality of memories (column 4, lines 26-27, memory modules), each of said processing units and memories being in communication with one another (column 4, lines 33-37) and wherein the total memory capacity of the chip is divided substantially equally between each of said processing layers (column 4, lines 20-30).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parameswaran Nair et al. as applied to claim 1 above, and further in view of Chakrabarti et al. (US Patent Number: 6,807,167).

Regarding claim 6, Parameswaran Nair et al. do not disclose expressly wherein the interface comprises a UTOPIA-compatible interface. However, Chakrabarti et al. teach wherein the interface comprises a UTOPIA-compatible interface (column 3, lines 5-15). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a UTOPIA-compatible interface. One of ordinary skill in the art would have been motivated to perform such a modification to provide support for circuit switching and packet switching applications and for supporting multimedia applications (Chakrabarti et al., column 1, lines 30-45).

Regarding claim 7, Parameswaran Nair et al. do not disclose expressly wherein the interface comprises a time division multiplex-compatible interface. However, Chakrabarti et al. teach wherein the interface comprises a time division multiplex-compatible interface (column 3, lines 5-15). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a UTOPIA-compatible interface. One of ordinary skill in the art would have been motivated to

perform such a modification to provide support for circuit switching and packet switching applications and for supporting multimedia applications (Chakrabarti et al., column 1, lines 30-45).

Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parameswaran Nair et al. as applied to claims 1 and 13 respectively above, and further in view of Hudepohl et al. (US Patent Number: 6,754,804).

Regarding claims 8 and 17, Parameswaran Nair et al. teach the limitations as set forth under claims 1 and 13 respectively above. However, Parameswaran Nair et al. do not disclose expressly wherein at least one processing layer includes a processing unit performing echo cancellation functions on received data and a processing unit performing encoding or decoding functions on received data and wherein said echo cancellation and encoding or decoding functions are performed in a pipelined manner. Hudepohl et al. teach wherein at least one processing layer includes a processing unit performing echo cancellation functions on received data and a processing unit performing encoding or decoding functions on received data and wherein said echo cancellation and encoding or decoding functions are performed in a pipelined manner (column 24, lines 40-60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use systems with multiple processing units and to perform tasks on a pipelined manner. One of ordinary skill in the art would have been motivated to do so because it is well known in the art that utilizing multiple processing units and performing tasks in a pipelined manner increases overall system performance.

Claim 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parameswaran Nair et al. as applied to claim 1 above, and further in view of Ehlig et al. (US Patent Number: 6,134,578).

Regarding claim 9, Parameswaran Nair et al. do not disclose expressly wherein the processing unit designed to perform encoding or decoding functions comprises an arithmetic and logic unit, multiply and accumulate unit, barrel shifter, and normalization unit. However, Ehlig et al. teach a processing unit comprising an arithmetic and logic unit (column 7, lines 37-43), multiply (column 9, lines 5-10) and accumulate unit (column 7, lines 25-35), barrel shifter (column 9, lines 45-65), and normalization unit (column 15, lines 27-41). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use processing units comprising an arithmetic and logic unit, multiply and accumulate unit, barrel shifter, and normalization unit. One of ordinary skill in the art would have been motivated to do so because it provides performance improvement over general purpose microprocessors to allow its use in real-time applications, such as speech and image processing (Ehlig et al., column 2, lines 1-35).

Regarding claim 10, Parameswaran Nair et al. do not disclose expressly wherein the processing unit additionally performs voice activity detection and tone signaling functions. However, Ehlig et al. teach wherein the processing unit additionally performs voice activity detection and tone signaling functions (column 26, lines 36-46, column 27, lines 1-15). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to perform voice activity detection and tone signaling

functions. One of ordinary skill in the art would have been motivated to do so because it allows its use in real-time applications, such as speech and image processing (Ehlig et al., column 2, lines 1-35).

Regarding claim 11, the combination of Parameswaran Nair et al. and Ehlig et al. teaches the limitations as set forth under claim 10 above. Furthermore, Ehlig et al. teach wherein the processing unit comprises a plurality of single-cycle multiply and accumulate units operating with an address generation unit and an instruction decoder (column 18, lines 1-35).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David G. Cervetti whose telephone number is (571) 272-5861. The examiner can normally be reached on Monday-Friday 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on (571)272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DGC

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100